FIG.1 Related Art

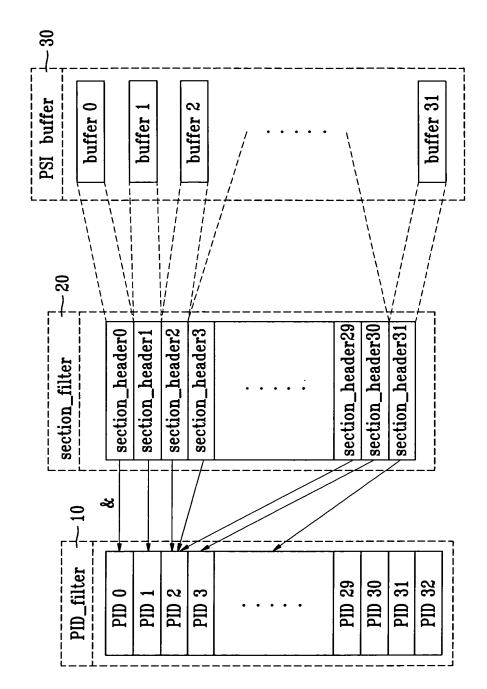
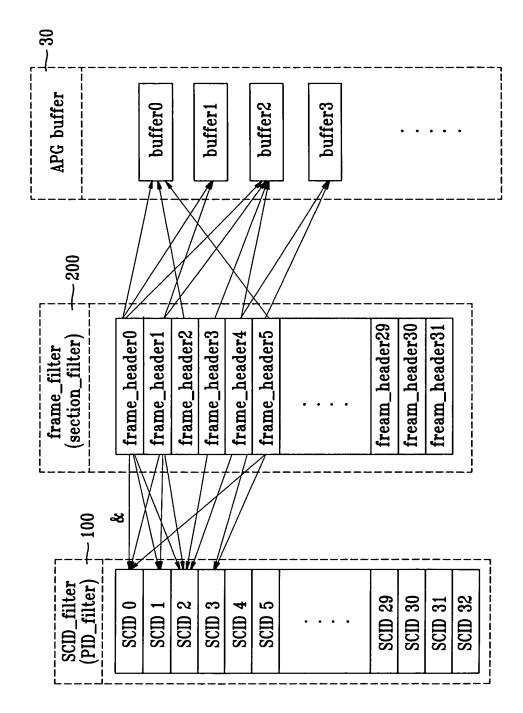


FIG.2



## FIG.3

frema_header 0	SCID_number (5 bits)	SCID_number SCID_number (5 bits) (5 bits)	SCID_number (5 bits)	SCID_number mask_bits
frema_header 1	$\begin{array}{c} \operatorname{ex} ) 0 \times 0 \\ \operatorname{SCID\_number} \\ (5 \text{ bits}) \\ \operatorname{ex} ) 0 \times 1 \end{array}$	$\begin{array}{c} \text{ex})0 \times 1 \\ \text{SCID\_number} \\ \text{(5 bits)} \\ \text{ex})0 \times 2 \end{array}$	SCID_number (5 bits) ex)None	SCID_number mask_bits (3 bits)
frema_header 2	SCID_number $(5 \text{ bits})$ $ex)0\times0$	SCID_number (5 bits) ex)None	SCID_number (5 bits) ex)None	SCID_number mask_bits (3 bits)
frema_header 3	SCID_number (5 bits) $ex)0 \times 2$	SCID_number (5 bits) ex)None	SCID_number (5 bits) ex)None	SCID_number mask_bits (3 bits)
frema_header 4	SCID_number (5 bits) $ex)0\times2$	SCID_number (5 bits) $ex)0 \times 3$	SCID_number (5 bits) ex)None	SCID_number mask_bits (3 bits)

frema_header 30	$\begin{array}{c c} \text{SCID\_number} & \\ \text{(5 bits)} \\ \text{ex)} \\ \text{0} \times 7 \end{array}$	SCID_number $(5 \text{ bits})$ $ex)0 \times 15$	SCID_number   SCID_number (5 bits) (5 bits) ex) $0 \times 15$ ex)None	SCID_number mask_bits (3 bits)
frema_header 31	SCID_number S $(5 \text{ bits})$ $ex)0 \times 14$	SCID_number $(5 \text{ bits})$ ex $)0 \times 15$	$\begin{array}{c c} \text{SCID\_number} & \text{SCID\_number} \\ (5 \text{ bits}) & (5 \text{ bits}) \\ \text{ex})0 \times 15 & \text{ex})0 \times 1a \end{array}$	SCID_number mask_bits (3 bits)

FIG.4

	31	30	29		5	4	3	2	1	0
scid0	0	0	0		1	0	0	1	0	1
	31	30	29		5	4	3	2	1	0
scid1	0	0	0		0	0	0	0	1	1
				•						
				: :						
	31	30	29		5	4	3	2	1	0
scid30	0	0	0	• • • • •	0	1	0	0	1	0
	31	30	29		5	4	3	2	1	0
scid31	0	0	0		1	0	0	0	0	1

FIG.5

Frame_start_point (start address of buffer)	Frame_start_point (end address of buffer)	Matched SCID_number	Matched frame_header _number
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